IN THE SPECIFICATION:

Please replace paragraphs 0028, and 0033, as follows:

[0028] The main memory 116 could be one or a combination of memory devices, including Random Access Memory, nonvolatile or backup memory, (*e.g.*, programmable or Flash memories, read-only memories, etc.). In addition, memory 116 may be considered to include memory physically located elsewhere in a computer system 110, for example, any storage capacity used as virtual memory or stored on a mass storage device or on another computer coupled to the computer system 110 via bus ~~128~~ 130.

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[0033] Figure 3 illustrates one embodiment of a cache purge instruction 128 used to purge a cache line addressed in field "RA" 310. Illustratively, the cache purge instruction 128 is an X-form PowerPC instruction 128 and the opcode 302 may be any notation recognized by a processor to execute the instruction. For example, the opcode ~~300~~ 302 may be represented by a hexadecimal notation. The field "M" contains information regarding which processor(s) and their associated caches will be updated and may contain a value equal to "0" or "1". For example, if the field "M" 304 equals "0", then the processor and its associated cache referenced by a processor number stored in field "RB" 312 is updated. Further, if the processor number stored in field "RB" 312 is the processor that is executing the instruction 128, then all processors and their associated caches are updated. If field "M" 304 equals "1", the processor chosen to be updated is determined based on the processor history 212 shown in Figure 2. Referring back to Figure 3, the field "H" 308 indicates the cache level that is to be updated and may contain any numerical value representative of a level of cache. As an illustration, if field "H" contains "0" then the level one (L1) cache is updated and so on. The field "P" 306 contains a value that indicates under what circumstances each processor in the system performs an update write to its cache or caches while updating the state field 208 of the cache line 202 in the cache directory 200. As an illustration, if field "P" 306 equals "0", then all caches are updated and the state field 208 of the cache line addressed in field "RA" 310 is marked as shared. If field "P" equals "1", then the state of only one cache line at a designated processor is updated and marked exclusive while

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A2 the issuing processor marks the cache line temporarily invalid. If field "P" equals "2" then all caches are updated and the cache line state is marked as temporarily invalid.